This application claims priority as a divisional to U.S. Patent Application Serial No. 09/207,343 filed December 8, 1998.

IN THE CLAIMS:

Please cancel claims 1–15 without prejudice. Please amend the remaining claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

16. (unchanged) A method for providing video motion compensation comprising the steps of:

receiving one or more prediction blocks;

receiving one or more instructions;

receiving one or more error terms; and

utilizing at least the one or more prediction blocks and the one or more error terms as directed by the one or more instructions to produce a decoded macroblock.

17. (unchanged) A method for providing video motion compensation comprising the steps of:

receiving an instruction and writing the instruction to an instruction queue;

moving the instruction from the instruction queue to an execution unit if the execution unit is not full;

receiving an error term and writing the error term to an error memory;

executing the instruction in the execution unit if the instruction is not a write instruction; and

if the instruction in the execution unit is a write instruction, waiting until the error memory is full, and then utilizing at least all the error terms stored in the error memory and one or more prediction blocks stored in a merge memory to produce a decoded macroblock.

18. (unchanged) The method for providing video motion compensation as recited in claim 17, wherein the step of executing the instruction in the execution unit if the instruction is not a write instruction further comprises the step of if the instruction in the execution unit is a load instruction, reading a prediction block from a reference buffer, utilizing at least the prediction block and a half pixel filter to produce a filtered prediction block, and writing the filtered prediction block to a merge memory.

19. (unchanged) The method for providing video motion compensation as recited in claim 17, wherein the step of executing the instruction in the execution unit if the instruction is not a write instruction further comprises the step of if the instruction in the execution unit is a merge instruction, reading a prediction block from a reference buffer, utilizing at least the prediction block and a half pixel filter to produce a filtered prediction block, and merging the filtered prediction block with one or more previously filtered prediction blocks.

20. (unchanged) A system for providing video motion compensation comprising:

a video decoder configured to produce one or more instructions and one or more error terms;

a picture memory; and

a digital video processor comprising an error memory communicably coupled to the video decoder, a half pixel filter communicably coupled to the picture memory, a merge memory communicably coupled to the half pixel filter, a controller communicably coupled to the video decoder, the error memory, the merge memory and the half pixel filter, a sum unit communicably coupled to the error memory, the merge memory and the picture memory, and the controller executing the one or more instructions to provide motion compensation.

21. (unchanged) The system for providing video motion compensation as recited in claim 20, further comprising:

an error buffer communicably coupled between the error memory and the video decoder;

an instruction buffer communicably coupled between the controller and the video decoder;

a reference buffer communicably coupled between the half pixel filter and the picture memory; and

a display buffer communicably coupled between the sum unit and the picture memory.

22. (unchanged) The system for providing video motion compensation as recited in claim 21, wherein the error memory, the merge memory, the picture memory, the error buffer, the instruction buffer, the display buffer and the reference buffer are static random access memory.

Please add the following new claims:

23. (newly added) A digital video system comprising:

a DVD drive;

a track buffer communicably coupled to the DVD drive;

a demultiplexer communicably coupled to the track buffer

a video input buffer communicably coupled to the demultiplexer;

a digital video decoder communicably coupled to the video input buffer, the digital video decoder utilizing at least an encoded video data stream to produce one or more output streams, the one or more output streams comprising at least a set of motion compensation instructions and a set of error terms;

a digital video processor coupled to the digital video decoder, the digital video processor providing motion compensation using the set of motion compensation instructions and the set of error terms;

a mixer communicably coupled to the digital video processor; and

a video renderer communicably coupled to the mixer.

24. (newly added) The digital video system as recited in claim 23, wherein the digital video processor further comprises:

an error memory and a merge memory;

a half pixel filter communicably coupled to the merge memory;

a controller communicably coupled to the error memory, the merge memory and the half pixel filter, the controller executing the motion compensation instructions; and

a sum unit communicably coupled to the error memory and the merge memory.

25. (newly added) The digital video system as recited in claim 24, wherein the digital video processor further comprises:

an error buffer communicably coupled to the error memory;

an instruction buffer communicably coupled to the controller;

a reference buffer communicably coupled to the half pixel filter; and

a display buffer communicably coupled to the sum unit.

26. (newly added) The digital video system as recited in claim 24, wherein the controller further comprises:

an instruction queue;

an execution unit communicably connected to the instruction queue and the error memory; and

a motion compensation state machine communicably connected to the execution unit, the half pixel filter and the merge memory.

27. (newly added) The digital video system as recited in claim 24, wherein the sum unit uses at least one of the error terms stored in the error memory with one or more filtered prediction blocks stored in the merge memory to produce a decoded macroblock.

28. (newly added) The digital video system as recited in claim 24, wherein the half pixel filter performs vertical and horizontal half-pixel interpolation on a block as dictated by a motion vector.

29. (newly added) The method as recited in claim 16, further comprising:

receiving the one or more prediction blocks, the one or more instructions, and the one or more error terms from a video decoder capable of selectively formulating the instructions.

30. (newly added) The method as recited in claim 16, further comprising:

filtering the one or more prediction blocks with a half pixel filter performing vertical and horizontal half-pixel interpolation on each prediction block as dictated by a motion vector within an instruction associated with the prediction block; and

utilizing each of the one or more error terms with an associated filtered prediction block from the one or more prediction blocks filtered by the half pixel filter to produce the decode macroblock.

31. (newly added) The method as recited in claim 16, wherein the step of receiving one or more instructions further comprises:

receiving at least one each motion compensation instruction comprising an instruction descriptor followed by one or more data descriptors, the instruction descriptor comprising at least a first data field and a second data field, the first data field indicating an operation to be performed and the second data field indicating how many of the data descriptors follow the instruction descriptor, each data descriptor comprising a third data field and a fourth data field, the third data field indicating a memory address of a first word in a prediction block associated with the at least one motion compensation instruction and the fourth data field indicating a number of words in the prediction block.

32. (newly added) The method as recited in claim 16, further comprising:

utilizing the one or more instructions to control a motion compensation state machine employed to produce the decoded macroblock.

33. (newly added) The method as recited in claim 16, further comprising:

storing the one or more received error terms within an error memory communicably coupled to a controller for executing the one or more instructions.

34. (newly added) The method as recited in claim 16, further comprising:

filtering the one or more prediction blocks with a half pixel filter performing vertical and horizontal half-pixel interpolation on each prediction block as dictated by a motion vector within an instruction associated with the prediction block; and

storing filtered prediction blocks within a merge memory communicably coupled to a controller for executing the one or more instructions.

35. (newly added) The method as recited in claim 16, further comprising:

storing the one or more instructions within an instruction queue communicably coupled to a controller for executing the one or more instructions.